

## CLAIM AMENDMENTS

1           1. (previously presented) A method of converting a  
2 silicon on insulator (SOI) substrate into a strained SOI substrate,  
3 the method comprising the steps of:

4           providing an SOI substrate having a thin silicon layer  
5 and an insulator;

6           providing at least one first epitaxial relaxing layer on  
7 the SOI-substrate,

8           producing a defect region in a layer above the silicon  
9 layer of the SOI-substrate, and

10          relaxing the first layer by a thermal treatment in an  
11 inert atmosphere to simultaneously strain the silicon layer of the  
12 SOI-substrate via dislocation mediated strain transfer and to  
13 produce the strained silicon layer directly on the insulator.

1           2. (previously presented) The method according to claim  
2 1, further comprising the step of

3           forming defects that give rise to relaxation of at least  
4 one neighboring layer of the layer which is to be strained.

1           3. (previously presented) The method according to claim  
2 1, further comprising the step of

3           subjecting the layer structure for relaxation to a  
4 thermal treatment and/or oxidation.

1           4. (previously presented) The method according to  
2 claim 1, further comprising the step of  
3           depositing the first layer upon the silicon layer to be  
4 strained.

1           5. (currently amended) The method according to claim 4  
2 wherein the first layer has a different degree of ~~stress~~ strain  
3 than the silicon layer to be strained.

4           6. (previously presented) The method according to claim  
5 4 wherein the defect region is produced in the first layer.

7 - 9. (canceled)

1           10. (currently amended) The method according to claim 1  
2 wherein two neighboring layers of the layer to be strained have  
3 other degrees of ~~stress~~ strain than the layer to be strained.

1           11. (previously presented) The method according to  
2 claim 1 wherein a plurality of layers are relaxed.

1           12. (previously presented) The method according to  
2 claim 1 wherein a plurality of layers to be strained have strain  
3 transferred to them.

1           13. (previously presented) The method according to  
2 claim 1, further comprising the step of  
3           depositing on the first layer epitaxially at least one  
4 second layer with a different lattice structure.

1           14. (previously presented) The method according to  
2 claim 13 wherein the defect region is produced in the second layer.

1           15. (previously presented) The method according to  
2 claim 1 wherein on the layer to which strain is to be transferred  
3 at least one graded layer is deposited as the first layer.

1           16. (previously presented) The method according to  
2 claim 15 wherein at the region of the layer to be strained, the  
3 graded layer has a degree of strain that is different from that of  
4 the layer to be strained.

1           17. (previously presented) The method according to  
2 claim 15, further comprising the step of  
3           producing a defect region in the graded layer.

4           18. (previously presented) The method according to  
5 claim 1, further comprising the step of  
6           depositing an epitaxial layer structure comprising a  
7 plurality of layers on the substrate.

19. (canceled)

1           20. (currently amended) The method according to claim 1  
2    [[9]] wherein the thermal treatment is done at a temperature  
3    between 550 degrees and 1200 degrees C.

1           21. (currently amended) The method according to claim 1  
2    [[9]] wherein the thermal treatment is done at a temperature  
3    between 700 degrees and 980 degrees C.

22 - 23. (canceled)

1           24. (previously presented) The method according to  
2    claim 1 wherein the relaxation is carried out over a limited region  
3    of a layer.

4           25. (previously presented) The method according to  
5    claim 1, further comprising the step of  
6    applying a mask.

26 - 27. (canceled)

1           28. (previously presented) A method of converting a  
2 silicon on insulator (SOI) substrate into a strained SOI substrate,  
3 the method comprising the steps of:

4           providing an SOI substrate having a thin silicon layer  
5 and an insulator;

6           providing at least one first epitaxial relaxing layer on  
7 the SOI-substrate,

8           producing a defect region in a layer above the silicon  
9 layer of the SOI-substrate by ion implantation of hydrogen ions or  
10 helium ions with a dose of  $3 \times 10^{15}$  to  $4 \times 10^{16}$  cm<sup>-2</sup>, and

11           relaxing the layer above the silicon layer by a thermal  
12 treatment to simultaneously strain the silicon layer of the SOI-  
13 substrate via dislocation mediated strain transfer and to produce  
14 the strained silicon layer directly on the insulator.

29 - 34. (canceled)

1           35. (previously presented) The method according to  
2 claim 13, further comprising out the step of

3           carrying out two implantations to produce two defect  
4 regions in the first layer and in the second layer.

1           36. (previously presented) The method according to  
2 claim 28, further comprising the step of

3           tilting the substrate during the ion implantation at an  
4   angle greater than 7°.

37. (canceled)

1           38. (previously presented) The method according to  
2   claim 1 wherein the defect region is produced by a change in the  
3   temperature during the formation of one of the layers.

1           39. (previously presented) The method according to  
2   claim 1 wherein the defects are produced in a Si-C layer by thermal  
3   treatment.

40 - 41. (canceled)

1           42. (previously presented) The method according to  
2   claim 1 wherein a silicon surface layer of the SOI substrate is the  
3   layer to be strained and the SiO<sub>2</sub> of the SOI substrate forms the  
4   insulator of the substrate.

1           43. (previously presented) The method according to  
2   claim 1 wherein an SIMOX or BESOI substrate is selected as a base  
3   structure for the substrate.

1           44. (previously presented) The method according to  
2 claim 1, further comprising the step of  
3           selecting a silicon on sapphire as a base structure for  
4 the substrate.

1           45. (previously presented) The method according to  
2 claim 1 wherein the layer neighboring the silicon layer becomes  
3 viscous at a temperature required for the relaxation.

46 - 47. (canceled)

1           48. (previously presented) The method according to  
2 claim 1 Si-Ge or Si-Ge-C or Si-C as the material for the first  
3 layer which is deposited on the layer to be strained.

49. (canceled)

1           50. (previously presented) The method according to  
2 claim 13 wherein silicon as the material for the second layer which  
3 is deposited upon the first layer.

1           51. (previously presented) The method according to  
2 claim 15, further comprising the step of  
3           selecting Si-Ge as the material for a graded layer.

1           52. (previously presented) The method according to  
2 claim 51 wherein the germanium concentration in the graded layer  
3 decreases from the interface with the layer to be strained to the  
4 surface of the graded layer.

1           53. (previously presented) The method according to  
2 claim 15 wherein the germanium concentration in a Si-Ge layer at  
3 the interface with the layer to be strained is 100 percent.

54. (canceled)

1           55. (previously presented) A method of converting a  
2 silicon on insulator (SOI) substrate into a strained SOI substrate,  
3 the method comprising the steps of:

4           providing an SOI substrate having a thin silicon layer  
5 and an insulator;

6           growing at least one first epitaxial relaxing layer on  
7 the SOI-substrate,

8           producing a defect region in a layer above the silicon  
9 layer of the SOI-substrate,

10          relaxing the layer above the silicon layer by a thermal  
11 treatment to simultaneously strain the silicon layer of the SOI-  
12 substrate via dislocation mediated strain transfer and to produce  
13 the strained silicon layer directly on the insulator, the

14 dislocation density after growth amounting to less than  $10^5 \text{ cm}^{-2}$ ,  
15 and

16 selecting a total layer thickness of the layer structure  
17 that during growth of the epitaxial layer it does not substantially  
18 relax.

1 56. (previously presented) The method according to  
2 claim 1 wherein a layer to be strained has a thickness  $d_3$  in the  
3 range of 1 to 50 nanometers.

4 57. (previously presented) The method according to  
5 claim 1 wherein the silicon layer to be strained has a thickness  $d_3$   
6 in the range of 5 to 30 nanometers.

7 58. (previously presented) The method according to  
8 claim 57 wherein the first layer has a thickness  $d_4$  close to a  
9 critical layer thickness for pseudomorphic growth.

1 59. (previously presented) The method according to  
2 claim 58 wherein a layer thickness ratio  $d_4/d_3$  is greater than about  
3 10.

1 60. (previously presented) The method according to  
2 claim 13 wherein the second layer has a thickness  $d_5 = 50$  nanometer  
3 to 1000 nanometer.

1           61. (previously presented) The method according to  
2 claim 13 wherein the second layer has a thickness  $d_5 = 300$   
3 nanometer to 500 nanometer.

1           62. (previously presented) The method according to  
2 claim 1 wherein the layer to be strained is locally strained.

1           63. (previously presented) The method according to  
2 claim 62 wherein the layer to be strained is locally strained in  
3 regions which are vertical in a plane with the defect region.

1           64. (previously presented) The method according to  
2 claim 13 wherein the defect region is produced at a spacing of 50  
3 nanometers to 500 nanometers from the layer to be relaxed.

1           65. (previously presented) The method according to  
2 claim 1 wherein the defect region is at a spacing of 50 nanometers  
3 to 100 nanometers above the first layer on the layer to be  
4 strained.

1           66. (previously presented) The method according to  
2 claim 13, further comprising the step of  
3 removing the first and second layers after producing the  
4 strained layer or after producing a strained region.

1           67. (previously presented) The method according to  
2 claim 1 wherein wet chemical material-selective etching is used.

3           68. (previously presented) The method according to  
4 claim 67, further comprising the step of  
5 etching trenches in the depth of the silicon and  
6 epitaxial layers.

1           69. (previously presented) The method according to  
2 claim 68, further comprising the step, after producing the etched  
3 trenches, of  
4 relaxing the first layer or a further layer by a thermal  
5 treatment.

1           70. (previously presented) The method according to  
2 claim 68, further comprising the step of  
3 filling the trenches with insulating material to produce  
4 shallow trench insulation.

1           71. (previously presented) The method according to  
2 claim 1, further comprising the step of  
3 carrying out at least one further thermal treatment for  
4 relaxation of at least one layer.

1           72. (previously presented) The method according to  
2 claim 1 wherein a strained layer or an unstrained layer are  
3 produced with a surface roughness of less than 1 nanometer.

1           73. (previously presented) The method according to  
2 claim 72 wherein a surface roughness of the layer is further  
3 reduced by the growth of a thermal oxide thereon.

1           74. (previously presented) The method according to  
2 claim 1, further comprising the step of  
3           producing on a strained region of the layer an n- and/or  
4 p- MOSFET.

1           75. (previously presented) The method according to  
2 claim 1, further comprising the step of  
3           depositing a further epitaxial layer comprising silicon  
4 or silicon/germanium or an Si-Ge-C layer or a germanium layer.

1           76. (previously presented) The method according to  
2 claim 1, further comprising the step of  
3           producing on a strained silicon-germanium region  
4 p-MOSFETs as a further epitaxial layer or as a nonrelaxed layer  
5 structures.

1           77. (previously presented) The method according to  
2 claim 1, further comprising the step of  
3           producing bipolar transistors on unstrained regions of  
4 the layer to be strained.

1           78. (previously presented) The method according to  
2 claim 77 wherein for producing a bipolar transistor, a silicon-  
3 germanium layer is applied.

1           79. (previously presented) The method according to  
2 claim 1, wherein the steps of claim 1 are carried out a plurality  
3 of times.

80 - 98. (canceled)

1           99. (new) The method according to claim 19 wherein the  
2 thermal treatment is carried out in nitrogen.

3           100. (new) The method according to claim 28 wherein at  
4 least two implantations are carried out.

1           101. (new) The method according to claim 100 wherein a  
2 hydrogen implantation is carried out in combination with a helium  
implantation.

1           102. (new) The method according to claim 32 wherein  
2   between two implantations a thermal treatment is carried out.

3           104. (new) The method according to claim 1 wherein the  
4   total layer thickness of the layer structure is so selected that  
5   during growth of the epitaxial layer it does not produce any  
6   noticeable relaxation.